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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/684,102	10/09/2003	Chandan Mathur	1934-11-3	3022

7590 03/02/2006

Bryan A. Santarelli
GRAYBEAL JACKSON HALEY LLP
Suite 350
155 - 108th Avenue NE
Bellevue, WA 98004-5901

EXAMINER	
ZALEPA, GEORGE D	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 03/02/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/684,102	MATHUR ET AL.	
	Examiner	Art Unit	
	George D. Zalepa	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 09 October 2003.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-27 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-27 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 3/12/05, 4/11/05, 6/19/05
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-27 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file:

a. Declaration as filed on 9 October 2003.

b. Information Disclosure Statements filed 18 March 2005, 11 April 2005, and 19 September 2005.

Information Disclosure Statement

3. The references listed in the Information Disclosure Statement submitted on 18 March 2005, 11 April 2005, and 19 September 2005 have been considered by the examiner (see attached PTO-1449).

Specification

4. The disclosure is objected to because of the following informalities: In numerous paragraphs, applicant uses the phrase "Serial No(s). ___". Applicant is requested to insert serial number of related patent application in place of underscores. Appropriate correction is required.

5. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: Peer-vector system utilizing a host processor and pipeline accelerator for improved program performance.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-2, 5-8, and 16 are rejected under 35 U.S.C. 102(b) as being anticipated by Ullner (US Pat. No. 6,112,288).

8. Regarding **independent claim 1,**

9. Ullner discloses *a peer-vector machine, comprising: a host processor* [see Ullner, Fig. 2, element 15] *operable to execute a program* [see Ullner, Col. 2, lines 59-61 ("...executes server software...")], *and, in response to the program, operable to generate first host data* [see Ullner, Col. 12, lines 52-53; Examiner's note: It is clear that the host processor disclosed by Ullner selects data from the local disk thus generating host data to be sent to the pipeline accelerator.]*; and a pipeline accelerator* [see Ullner, Fig. 1, element 19] *coupled to the host processor* [see Ullner, Col. 2, line 67; Col. 2, lines 1-2] *and operable to receive the first host data* [see Ullner, Col. 3, lines 28-33; Examiner's note: Ullner discloses data being sent to the controller, it would have been inherent that said data is then sent to the pipeline accelerator] *and to generate first pipeline data from the first host data* [see Ullner, Col. 3, lines 21-27; "...collect all remaining result data and return that data to the host."].

10. Regarding **claim 2,**

11. Ullner discloses *the peer-vector machine of claim 1 wherein the host processor is further operable to: receive second data; and generate the first host data from the second data* [see Ullner, Col. 2, lines 58-60; Examiner's note: Ullner discloses the use of a host computer/processor comprising a COTS computer. It would be inherent that a standard processor would at least be capable of processing instructions sequentially. Thus, upon executing software (Col. 2, lines 59-61), it would have been inherent that multiple instructions would have been executed, thus allowing a second data (instruction) to generate the host data.].

12. Regarding **claim 5,**

13. Ullner discloses *the peer-vector machine of claim 1, further comprising: an interface memory coupled to the host processor and to the pipeline accelerator* [see Ullner, Fig. 3, element 27] *and having a first memory section* [see Ullner, Fig. 3, element 40b, "FIFO"]*; wherein the host processor is operable to, store the first host data in the first memory section* [see Ullner, Col. 3, lines 9-13; Examiner's note: The use of a FIFO by Ullner inherently implies that data is stored prior to being utilized by the accelerator.], *and provide the first host data from the first memory section to the pipeline accelerator* [Examiner's note: It would have been inherent that a FIFO buffer by definition of its architecture provides data to the pipeline accelerator.].

14. Regarding **claim 6**,

15. Ullner discloses *the peer-vector machine of claim 1, further comprising: an interface memory coupled to the host processor and to the pipeline accelerator and having first* [see Ullner, Fig. 3, element 40b] *and second memory sections* [see Ullner, Fig. 3, element 50]*; wherein the host processor is operable to, store the first host data in the first memory section* [see Ullner, Col. 3, lines 10-13; Examiner's note: The use of a FIFO by Ullner inherently implies that data is stored prior to being utilized by the accelerator.], *provide the first host data from the first memory section to the pipeline accelerator* [Examiner's note: It would have been inherent that a FIFO buffer (40b) by definition provides data to the pipeline accelerator.], *receive the first pipeline data from the pipeline accelerator, store the first pipeline data in the second memory section* [see Ullner, Col. 3, lines 6-8], *retrieve the first pipeline data from the second memory section to the host processor* [Examiner's note: It would have been inherent that a FIFO buffer (52) by definition provides data to the host processor.], *and process the first pipeline data* [see Ullner, Col. 3, lines 21-27].

16. Regarding **claim 7**,

17. Ullner discloses *the peer-vector machine of claim 1 wherein the host processor is operable to configure the pipeline accelerator* [see Ullner, Col. 3, lines 59-63].

18. Regarding **claim 8**,

19. Ullner discloses *the peer-vector machine of claim 1 wherein the pipeline accelerator comprises a programmable-logic integrated circuit* [see Ullner, Col. 1, lines 8-10].

20. Regarding **independent claim 16**,

21. Ullner discloses *a system, comprising: a device operable to generate raw data* [see Ullner, Col. 2, lines 53-56; Examiner's note: Ullner discloses a host computer receiving data from multiple clients (11), it is assumed that the data received from the client computers is considered raw data to be utilized by the host processor and subsequently the accelerator.]*; a host processor coupled to the device* [see Ullner, Fig. 2, element 15] *and operable to execute a program* [see Ullner, Col. 2, lines 59-61; Examiner's note: Ullner discloses data prepared by element 15 to be stored in a COTS disk before being sent to an accelerator. It would have been inherent that this data was created by the host processor in response to raw data being sent to the host processor by the client computers (Fig. 1, elements 11)], *and, in response to the program, operable to generate host data from the raw data* [see Ullner, Col. 12, lines 52-53; Examiner's note: It is clear that the host processor disclosed by Ullner selects data from the local disk thus generating host data to be sent to the pipeline accelerator.]*; and a pipeline accelerator coupled to the host processor* [see Ullner, Fig. 1, element 19] *and operable to receive the host data and to generate pipeline data from the host data* [see Ullner, Col. 3, lines 21-27].

22. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

23. Claims 1-4, 9-12, 18, 20-21, 23, 25, and 26 are rejected under 35 U.S.C. 102(e) as being anticipated by Snyder (US Pat. App. Pub. 2002/0087829).

24. Regarding **independent claim 1**,

25. Snyder discloses *a peer-vector machine, comprising: a host processor operable to execute a program* [see Snyder, Fig. 1, element 104; Para. 15, lines 6-7; Examiner's note: It would have been inherent to one of ordinary skill in the art at the time of invention that a DSP core would have the capabilities to execute a program stored in memory (such as memory 108 in Fig. 1 of Snyder)], *and, in response to the program, operable to generate first host data* [Examiner's note: Snyder discloses a digital signal processor that would have been inherently able to generate data based on the execution of an instruction.]*; and a pipeline accelerator* [see Snyder, Fig. 2] *coupled to the host processor* [see Snyder, Fig. 1, element 114; Examiner's note: Element 114 refers to a bus utilized to connect the SFU (accelerator) to the DSP Core (host processor).] *and operable to receive the first host data and to generate first pipeline data from the first host data* [see Snyder, Para. 0018, lines 2-5; Examiner's note: the SFU disclosed by Snyder receives the data to be processed from the DSP core and processes it accordingly (i.e., with an FFT, LMS, or similar filter (para. 0019)), thus generating a processed pipeline data from the host data.].

26. Regarding **claim 2**,

27. Snyder discloses *the peer-vector machine of claim 1 wherein the host processor is further operable to: receive second data; and generate the first host data from the second data* [see Snyder, Para. 0002, lines 1-5; Examiner's note: It would have been inherent to one of ordinary skill in the art at the time of invention that a DSP core is capable and utilized to execute a stream of instructions rather than only one instruction.].

28. Regarding **claim 3**,

29. Snyder discloses *the peer-vector machine of claim 1 wherein the host processor is further operable to: receive the first pipeline data from the pipeline accelerator; and process the first pipeline data* [see Snyder, Para. 0019; Examiner's note: In this paragraph Snyder discloses some of the functions the accelerator can perform. Given the use of a DSP core and the functions performed by the accelerator, it would have been inherent to one of ordinary skill in the art at the time of invention that data processed by the accelerator (such as an FFT operation) would have been processed due to the need for the results by the DSP core for an application such as cascaded filters.].

30. Regarding **claim 4**,

31. Snyder discloses *the peer-vector machine of claim 1 wherein the host processor is further operable to: receive the first pipeline data from the pipeline accelerator; and generate the first host data from the first pipeline data* [see Snyder, Para. 0019; Examiner's note: In this paragraph Snyder discloses some of the functions the accelerator can perform. Given the use of a DSP core and the functions performed by the accelerator, it would have been inherent to one of ordinary skill in the art at the time of invention that data processed by the accelerator (such as an FFT operation) would have been processed due to the need for the results by the DSP core for an application such as cascaded filters.].

32. Regarding **independent claim 9**,

33. Snyder discloses *a peer-vector machine, comprising: a pipeline accelerator* [see Snyder, Fig. 2] *operable to generate first pipeline data* [see Snyder, Para. 0018, lines 2-5; Examiner's note: the SFU disclosed by Snyder receives the data to be processed from the DSP core and processes it accordingly (i.e., with an FFT or LMS filter or the like (para. 0019)), thus generating a processed pipeline data from the host data.]*; and a host processor coupled to the pipeline accelerator and operable to execute a program* [see Snyder, Fig. 1, element 104; Para. 15, lines 6-7; Examiner's note: It would have been inherent to one of ordinary skill in the art at the time of invention that a DSP core would have the capabilities to execute a program stored in memory (such as memory 108 in Fig. 1 of Snyder)] *and, in*

response to the program, operable to receive the first pipeline data and to generate first host data from the first pipeline data [see Snyder, Para. 0019; Examiner's note: In this paragraph Snyder discloses some of the functions the accelerator can perform. Given the use of a DSP core and the functions performed by the accelerator, it would have been inherent to one of ordinary skill in the art at the time of invention that data processed by the accelerator (such as an FFT operation) would have been processed due to the need for the results by the DSP core for an application such as cascaded filters.].

34. Regarding **claim 10**,

35. Snyder discloses *the peer-vector machine of claim 9 wherein the pipeline accelerator is further operable to: receive second data; and generate the first pipeline data from the second data* [see Snyder, Para. 0002, lines 1-5; Examiner's note: It would have been inherent to one of ordinary skill in the art at the time of invention that a DSP core is capable and utilized to execute a stream of instructions rather than only one instruction. Furthermore, given the scope of the invention, it would have been inherent that the purpose of the invention was to utilize the SFU units to perform complex operations (such as a FFT or LMS), said operations very well likely to be juxtaposed. Thus, it would have been inherent that a second data stream would have been supplied by the DSP core to the SFU(s).].

36. Regarding **claim 11**,

37. Snyder discloses *the peer-vector machine of claim 9 wherein the pipeline accelerator is further operable to: receive the first host data from the host processor; and process the first host data* [see Snyder, Para. 0018, lines 2-5; Examiner's note: the SFU disclosed by Snyder receives the data to be processed from the DSP core and processes it accordingly (i.e., with an FFT of LMS filter (para. 0019)), thus generating a processed pipeline data from the host data. Although not explicitly stated, it would have been inherent that data from the DSP core would have been used as the input to the SFU(s) for data processing by said SFU(s).].

38. Regarding **claim 12**,

39. Snyder discloses *the peer-vector machine of claim 9 wherein the pipeline accelerator is further operable to: receive the first host data from the host processor; and generate the first pipeline data from the first host data* [see Snyder, Para. 0018, lines 2-5; Examiner's note: the SFU disclosed by Snyder receives the data to be processed from the DSP core and processes it accordingly (i.e., with an FFT or LMS filter or the like (para. 0019)), thus generating a processed pipeline data from the host data.].

40. Regarding **independent claim 18**,

41. Snyder discloses *a method, comprising: generating first host data by executing a program with a host processor; and generating first pipeline data from the first host data with a pipeline accelerator* [see Snyder, Para. 0018, lines 2-5; Examiner's note: the SFU disclosed by Snyder receives the data to be processed from the DSP core and processes it accordingly (i.e., with an FFT or LMS filter or the like (para. 0019)), thus generating a processed pipeline data from the host data.].

42. Regarding **claim 20**,

43. Snyder discloses *the method of claim 18 wherein generating the first host data comprises generating the first host data from the first pipeline data* [see Snyder, Para. 0019; Examiner's note: In this paragraph Snyder discloses some of the functions the accelerator can perform. Given the use of a DSP core and the functions performed by the accelerator, it would have been inherent to one of ordinary skill in the art at the time of invention that data processed by the accelerator (such as an FFT operation) would have been processed due to the need for the results by the DSP core for an application such as cascaded filters.].

44. Regarding **claim 21**,

45. Snyder discloses *the method of claim 18, further comprising generating second host data from the first pipeline data by executing the program with the host processor* [see Snyder, Para. 0019; Examiner's note: In this paragraph Snyder discloses some of the functions the accelerator can perform. Given the use of a DSP core and the functions performed by the accelerator, it would have been inherent

to one of ordinary skill in the art at the time of invention that data processed by the accelerator (such as an FFT operation) would have been processed due to the need for the results by the DSP core for an application such as cascaded filters.].

46. Regarding **independent claim 23**,

47. Snyder discloses *a method, comprising: generating first pipeline data with a pipeline accelerator; and generating first host data from the first pipeline data by executing a program with a host processor* [see Snyder, Para. 0019; Examiner's note: In this paragraph Snyder discloses some of the functions the accelerator can perform. Given the use of a DSP core and the functions performed by the accelerator, it would have been inherent to one of ordinary skill in the art at the time of invention that data processed by the accelerator (such as an FFT operation) would have been processed due to the need for the results by the DSP core for an application such as cascaded filters.].

48. Regarding **claim 25**,

49. Snyder discloses *the method of claim 23 wherein generating the first pipeline data comprises generating the first pipeline data from the first host data* [see Snyder, Para. 0018, lines 2-5; Examiner's note: the SFU disclosed by Snyder receives the data to be processed from the DSP core and processes it accordingly (i.e., with an FFT of LMS filter (para. 0019)), thus generating a processed pipeline data from the host data.].

50. Regarding **claim 26**,

51. Snyder discloses *the method of claim 23, further comprising generating second pipeline data from the first host data with the pipeline accelerator* [see Snyder, Para. 0018, lines 2-5; Examiner's note: it would have been inherent that a second pipeline data could have been created from a first host data in an instance of a loop in a program. Although not explicitly disclosed by Snyder, it is considered to have been well known at the time of invention.].

Claim Rejections - 35 USC § 103

52. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

53. Claims 13-15, 17, 19, 22, 24 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Snyder in view of Ullner.

54. Regarding **claim 13**,

55. Snyder discloses the limitations as stated in **independent claim 9**.

56. Snyder does not disclose *an interface memory coupled to the pipeline accelerator and to the host processor and having a first memory section; and wherein the host processor is operable to, store the first pipeline data from the pipeline accelerator in the first memory section, and retrieve the first pipeline data from the first memory section.*

57. Ullner does disclose *an interface memory coupled to the pipeline accelerator and to the host processor and having a first memory section* [see Ullner, Fig. 3, element 50]*; and wherein the host processor is operable to, store the first pipeline data from the pipeline accelerator in the first memory section* [see Ullner, Col. 3, lines 6-8]*, and retrieve the first pipeline data from the first memory section* [Examiner's note: It would have been obvious that a FIFO buffer (52) by definition provides data to the host processor.].

58. The advantage of utilizing a FIFO buffer to store incoming data to the pipeline accelerator would have been to allow the accelerator to finish processing results if the accelerator is busy before loading new data and commands into the accelerator. It can be seen in Fig. 3 of Ullner that FIFO 40b is connected to input to the accelerator(s), and due to the nature of a FIFO buffer, it would be obvious that the FIFO is operating in the above manner. Buffering input data to allow for processing completion

would have been a well known practice in the art at the time of invention, therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to utilize a buffering scheme, as proposed by Ullner, to store data that is unable to immediately be processed by the accelerator.

59. Regarding **claim 14**,

60. Snyder discloses the limitations as stated in **independent claim 9**.

61. Snyder does not disclose *an interface memory coupled to the pipeline accelerator and to the host processor and having first and second memory sections; wherein the host processor is operable to, store the first pipeline data from the pipeline accelerator in the first memory section, retrieve the first pipeline data from the first section, store the first host data in the second memory section, and provide the first host data from the second memory section to the pipeline accelerator; and wherein the pipeline accelerator is operable to process the first host data received from the second memory section.*

62. Ullner does disclose *an interface memory coupled to the pipeline accelerator and to the host processor and having first* [see Ullner, Fig. 3, element 50] *and second memory sections* [see Ullner, Fig. 3, element 40b]*; wherein the host processor is operable to, store the first pipeline data from the pipeline accelerator in the first memory section* [see Ullner, Col. 3, lines 6-8], *retrieve the first pipeline data from the first section, store the first host data in the second memory section* [see Ullner, Col. 3, lines 10-13], *and provide the first host data from the second memory section to the pipeline accelerator* [Examiner's note: It would have been obvious that a FIFO buffer (40b) by definition provides data to the pipeline accelerator.]*; and wherein the pipeline accelerator is operable to process the first host data received from the second memory section* [see Ullner, Col. 3, lines 21-27].

63. The advantage of utilizing a FIFO buffer to store incoming data to the pipeline accelerator would have been to allow the accelerator to finish processing results if the accelerator is busy before loading new data and commands into the accelerator. The use of the output FIFO would have been in similar spirit, however, would have functioned to allow for the host processor to finish processing pipeline data

before loading more processed data. It can be seen in Fig. 3 of Ullner that FIFO(s) 40b (52) are connected to the input/outputs of the accelerator(s), and due to the nature of a FIFO buffer, it would be obvious that the FIFO is operating in the above manner. Buffering input and output data to allow for processing completion would have been a well known practice in the art at the time of invention, therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to utilize a buffering scheme, as proposed by Ullner, to store data that is unable to immediately be processed by the accelerator or the host processor.

64. Regarding **claim 15**,

65. Snyder discloses the limitations as stated in **independent claim 9**.

66. Snyder does not disclose *the host processor* [being] *operable to configure the pipeline accelerator*.

67. Ullner does disclose *the host processor* [being] *operable to configure the pipeline accelerator* [see Ullner, Col. 3, lines 59-63].

68. Snyder discloses the use of programmable devices within the scope of the invention disclosed (see Snyder, para. 0005). However, Snyder does not disclose a method of programming the SFU(s). The advantage of using a programming scheme disclosed by Ullner would have been to allow a user to reconfigure the processing method of an accelerator based on any given application requested to be performed by the processor. Since Snyder discloses the use of a programmable device, it would have been obvious at the time of invention to allow the devices to be reprogrammed by an external program, such as the scheme proposed by Ullner.

69. Regarding **independent claim 17**,

70. Snyder discloses *a system, comprising: a pipeline accelerator coupled to the device and operable to generate pipeline data; and a host processor coupled to the pipeline accelerator and operable to*

execute a program and, in response to the program, operable to receive the pipeline data and to generate host data from the pipeline data.

71. Snyder does not disclose *a device operable to generate raw data; and generating pipeline data from the raw data.*

72. Ullner does disclose *a device operable to generate raw data; and generating pipeline data from the raw data* [see Ullner, Col. 2, lines 53-56; Examiner's note: Ullner discloses client computers sending data to a host processor which executes software to interpret and distribute data. The data sent from the client computers is considered to be raw data since it requires an intermediate processor to interpret it].

73. The advantage of being able to process raw data would have been

74. Regarding **claim 19**,

75. Snyder discloses the limitations as stated in **independent claim 18**.

76. Snyder does not disclose *receiving raw data; wherein generating the first host data comprises generating the first host data from the raw data.*

77. Ullner does disclose *receiving raw data; wherein generating the first host data comprises generating the first host data from the raw data* [see Ullner, Col. 2, lines 53-56; Examiner's note: Ullner discloses client computers sending data to a host processor which executes software to interpret and distribute data. The data sent from the client computers is considered to be raw data since it requires an intermediate processor to interpret it and send it to the accelerator for processing.].

78. The advantage of being able to process raw data would have been to allow for multiple clients to be able to submit processing orders to the accelerators as illustrated by Ullner with the use of multiple clients. By sending raw data, a variety of different clients could send data to the accelerator with the accelerator configured to process a standard format of data (a raw format). Furthermore, Snyder also does provide a means for accepting external communication data (para. 0038, lines 8-11), which could possibly be utilized for the acceptance of raw data. This advantage would have motivated one of ordinary skill in

the art at the time of invention to allow for the transmission of raw data via a bus (such as bus 428 in Fig. 3 of Snyder). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to combine the raw data methods taught by Ullner within the architecture disclosed by Snyder in Fig. 3.

79. Regarding **claim 22,**

80. Snyder discloses the limitations as stated in **independent claim 18**.

81. Snyder does not explicitly disclose *configuring the pipeline accelerator by executing the program with the host processor.*

82. Ullner does disclose *configuring the pipeline accelerator by executing the program with the host processor* [see Ullner, Col. 3, lines 59-63].

83. Snyder discloses the use of programmable devices within the scope of the invention disclosed (see Snyder, para. 0005). However, Snyder does not disclose a method of programming the SFU(s). The advantage of using a programming scheme disclosed by Ullner would have been to allow a user to reconfigure the processing method of an accelerator based on any given application requested to be performed by the processor. Since Snyder discloses the use of a programmable device, it would have been obvious at the time of invention to allow the devices to be reprogrammed by an external program, such as the scheme proposed by Ullner.

84. Regarding **claim 24,**

85. Snyder discloses the limitations as stated in **independent claim 23**.

86. Snyder does not disclose *receiving raw data; wherein generating the first pipeline data comprises generating the first pipeline data from the raw data.*

87. Ullner does disclose *receiving raw data; wherein generating the first pipeline data comprises generating the first pipeline data from the raw data* [see Ullner, Col. 2, lines 53-56; Examiner's note: Ullner discloses client computers sending data to a host processor which executes software to interpret

and distribute data. The data sent from the client computers is considered to be raw data since it requires an intermediate processor to interpret it and send it to the accelerator for processing.].

88. The advantage of being able to process raw data would have been to allow for multiple clients to be able to submit processing orders to the accelerators as illustrated by Ullner with the use of multiple clients. By sending raw data, a variety of different clients could send data to the accelerator with the accelerator configured to process a standard format of data (a raw format). Furthermore, Snyder also does provide a means for accepting external communication data (para. 0038, lines 8-11), which could possibly be utilized for the acceptance of raw data. This advantage would have motivated one of ordinary skill in the art at the time of invention to allow for the transmission of raw data via a bus (such as bus 428 in Fig. 3 of Snyder). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to combine the raw data methods taught by Ullner within the architecture disclosed by Snyder in Fig. 3.

89. Regarding **claim 27,**

90. Snyder discloses the limitations as stated in **independent claim 23.**

91. Snyder does not disclose *configuring the pipeline accelerator by executing the program with the host processor.*

92. Ullner does disclose *configuring the pipeline accelerator by executing the program with the host processor* [see Ullner, Col. 3, lines 59-63].

93. Snyder discloses the use of programmable devices within the scope of the invention disclosed (see Snyder, para. 0005). However, Snyder does not disclose a method of programming the SFU(s). The advantage of using a programming scheme disclosed by Ullner would have been to allow a user to reconfigure the processing method of an accelerator based on any given application requested to be performed by the processor. Since Snyder discloses the use of a programmable device, it would have

been obvious at the time of invention to allow the devices to be reprogrammed by an external program, such as the scheme proposed by Ullner.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to George D. Zalepa whose telephone number is (571) 272-6754. The examiner can normally be reached on Monday-Friday (alt. Friday off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie P. Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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George Zalepa
Examiner
Art Unit 2183
Randolph 2E74
Phone: (571) 272-6754

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100